#13 8-2-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaowei Deng	Docket No:	TI-29320
Serial No:	09/932,763	Conf. No:	5414
Examiner:	Daniel D. Chang	Art Unit:	2819
Filed:	08/16/2001		
For:	SILICON-ON-INSULATOR DYNAMIC LOGIC		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, DC 20231 on 7-18-03.

Ann Trent
Ann Trent

Assistant Commissioner of Patents
Washington, D. C. 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the rejection mailed April 18, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-3, 5-7, 9-11, and 13-15 were rejected. Claims 4, 8, 12, and 16 were objected to. Claims 1-16 are pending in this case. Claims 1-3, 5-7, 9-11, and 13-15 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

There are no amendments filed by the applicant after a final rejection.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The invention is a dynamic logic circuit on a SOI substrate. The circuit comprises a pull-down network (260 in Figure 4) comprising a plurality of series connect MOS transistors where at least one of the series connected transistors is a NMOS transistor and at least one is a PMOS transistor. The dynamic logic circuit also comprises a precharge circuit connected to a clock signal, the circuit supply voltage and the pull-down network. A ground switch circuit is connected to the clock signal and to the pull-down network, and the output node is taken from the common node of the pull-down network and the precharge circuit. Other embodiments of the instant invention include a pull-down network of series connected PMOS transistors (265 in Figure 5), a pull-down network of a plurality of parallel connected transistors with at least one PMOS transistor and one NMOS transistors (266 in Figure 6), and a pull-down network of parallel connected PMOS transistors (267 in Figure 7).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Are claims 1-3, 5-7, 9-11, and 13-15 properly rejected under 35 U.S.C. 103(a) as being unpatentable over the Hagihara patent (US2001/0001229A1).

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1-3, 5-7, 9-11, and 13-15 stand or fall together.

Arguments

1. Are claims 1-3, 5-7, 9-11, and 13-15 properly rejected under 35 U.S.C. 103(a) as being unpatentable over the Hagihara patent (US2001/0001229A1).

Appellants respectfully submit that claims 1-3, 5-7, 9-11, and 13-15 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over the Hagihara patent.

In his response on April 18, 2003 the examiner states that the Hagihara patent discloses a pull-down network in Figure 1 and also in paragraph [0005]. In addition to stating that a reference numeral 10 shows a logic circuit, paragraph [0005] also states that the logic circuit consists of n-type or p-type MOS transistors or both n-type and p-type MOS transistors. The examiner further states, "figure 1 does not specifically show the connections of n-type or p-type MOS transistors. The examiner is exactly correct in his interpretation of the Hagihara patent. It does not specifically show the connections of n-type or p-type MOS transistors, it only shows a logic circuit box with a reference numeral 10. The examiner then argues that the limitations of all the claims 1-3, 5-7, 9-11, and 13-15 are obvious over the Hagihara patent.

The examiner is directed to Graham et al. v. John Deere Co, 383 U.S. 1; 86 S. Ct. 684 for the criteria to be used in determining a proper obviousness rejection. As described in Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 228 USPQ 90 (Fed. Cir. 1985), the need for express Graham findings is important because of the "occasional tendency of district courts to depart from the Graham test, and from the statutory standard of nonobviousness that it helps determine, to the tempting but forbidden zone of hindsight." The examiner has presented a forbidden hindsight analysis.

In determining claims 1-3, 5-7, 9-11, and 13-15 obvious over the Hagihara patent the examiner has satisfied none of the criteria required under Graham. Under Graham there must be some suggestion to combine the Hagihara patent with other references. The examiner has presented no other references with which to combine the Hagihara patent. If it is indeed so "well known in the art" then the examiner should have had no trouble in finding other references with which to combine the Hagihara patent. The fact that the examiner has produced no such reference strongly suggests that no such references exist. Clearly under Graham simply stating that it is "well known" is not enough. If the examiner has references with which to combine the Hagihara patent then those references should be disclosed and presented. The examiner acquiesced to the appellants argument presented in an appeal brief mailed 3/12/03 that under the current interpretation of inherency claims 1-3, 5-7, 9-11, and 13-15 are not properly rejected under 35 U.S.C. 102(e) as being anticipated by the Hagihara patent (US2001/0001229A1). Given that the claims are not inherent in the Hagihara patent, it follows that the claims are also not obvious given the Hagihara patent without combining the Hagihara patent with other references that contain a suggestion to combine.

Claims 1-3, 5-7, 9-11, and 13-15 are clearly allowable over the Hagihara patent.

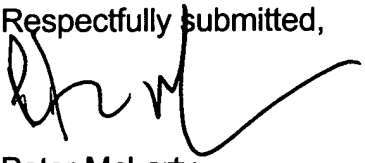
Conclusion

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of Claims 1-3, 5-7, 9-11, and 13-15 under 35 U.S.C. § 103(a) is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper,

including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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